WHAT IS CLAIMED IS:

1. A printed circuit board, comprising:

a substrate;

a first pair of vias in the substrate; and

a second pair of vias in the substrate; wherein

the first pair of vias is configured to convey a first signal pair and the second pair of vias is configured to convey a second signal pair;

the first pair of vias is positioned in a first plane,

the first plane is substantially equidistant from each via in the second pair of vias,

the second pair of vias is positioned in a second plane,

the second plane is substantially equidistant from each via in the first pair of vias.

2. The printed circuit board of claim 1, wherein

the first signal pair is a first differential signal pair, and

the second signal pair is a second differential signal pair.

3. The printed circuit board of claim 2, further comprising:

a plurality of Ball Grid Array (BGA) connectors, wherein

each via in the first pair of vias and the second pair of vias is coupled to a respective one of the plurality of BGA connectors.

4. The printed circuit board of claim 2, further comprising:

a first differential signal source coupled to each via in the first pair of vias, wherein

the first differential signal source is configured to generate the first differential signal pair conveyed by the first pair of vias.

5. The printed circuit board of claim 2, further comprising:

a plurality of isolation vias, wherein

the plurality of isolation vias substantially electromagnetically isolate the first pair of vias and the second pair of vias from a third pair of vias and a fourth pair of vias.

6. The printed circuit board of claim 5, wherein
the third pair of vias and the fourth pair of vias are each configured to convey a respective differential signal pair,
the third pair of vias is positioned in a third plane,
the third plane is substantially equidistant from each via comprised in the fourth pair of vias,
the fourth pair of vias is positioned in a fourth plane, and
the fourth plane is substantially equidistant from each via included in the third pair of vias.

7. The printed circuit board of claim 2, wherein
a skew of a first pair of traces is matched at a point at which the first pair of traces couples to the first pair of vias.

8. The printed circuit board of claim 7, wherein
a skew of a second pair of traces is matched at a point at which the second pair of traces couples to the second pair of vias.

9. The printed circuit board of claim 8, wherein
the first pair of traces are routed on a same layer as the second pair of traces.

10. The printed circuit board of claim 8, wherein
the first pair of traces are routed on an adjacent layer to the second pair of traces.

11. The printed circuit board of claim 2, wherein
the first pair of vias is configured to convey a positive differential signal and a negative differential signal;

the first pair of vias is positioned relative to the second pair of vias such that a crosstalk effect caused by the second signal pair on the positive differential signal reduces a crosstalk effect caused by the second signal pair of the negative differential signal.

12. The printed circuit board of claim 11, wherein
the first pair of vias is positioned relative to the second pair of vias such that a crosstalk effect caused by the second signal pair on the positive differential signal substantially cancels a crosstalk effect caused by the second signal pair of the negative differential signal.

13. The printed circuit board of claim 2, wherein
the first pair of vias is configured to convey the first differential signal pair at a data rate greater than 250 megabits per second.

14. A printed circuit board, comprising:
a substrate;
a first pair of vias in the substrate; and
a second pair of vias in the substrate, wherein
the first pair of vias is configured to convey a first signal pair comprising a first positive signal and a first negative signal,
the second pair of vias is configured to convey a second signal pair comprising a second positive signal and a second negative signal,
the first pair of vias is positioned relative to the second pair of vias such that a crosstalk effect caused by the first signal pair on the second positive signal reduces a crosstalk effect caused by the first signal pair on the second negative signal.

15. The printed circuit board of claim 14, wherein
the second pair of vias is positioned relative to the first pair of vias such that a crosstalk effect caused by the second signal pair on the first positive signal reduces a crosstalk effect caused by the second signal pair on the first negative signal.

16. The printed circuit board of claim 15, wherein
the first positive signal and the first negative signal are comprised in a first differential signal pair, and
the second positive signal and the second negative signal are comprised in a second differential signal pair.

17. The printed circuit board of claim 14, wherein
a skew of a first pair of traces is matched at a point at which the first pair of traces couples to the first pair of vias.

18. The printed circuit board of claim 17, wherein
a skew of a second pair of traces is matched at a point at which the second pair of traces couples to the second pair of vias.

19. The printed circuit board of claim 14, further comprising:
a plurality of Ball Grid Array (BGA) connectors, wherein
each via in the first pair of vias and the second pair of vias is coupled to a respective one of the plurality of BGA connectors.

20. A method, comprising:
conveying a first signal pair, wherein a first pair of vias convey the first signal pair; and
conveying a second signal pair, wherein a second pair of vias convey the second signal pair, wherein
the first pair of vias is positioned in a first plane,
the first plane is substantially equidistant from each via in the second pair of vias,
the second pair of vias is positioned in a second plane, and
the second plane is substantially equidistant from each via in the first pair of vias.

21. The method of claim 20, wherein

the first signal pair is a first differential signal pair, and
the second signal pair is a second differential signal pair.

22. The method of claim 21, wherein
the first pair of vias is coupled to a first pair of Ball Grid Array (BGA) connectors,
the second pair of vias is coupled to a second pair of BGA connectors, and
the method further comprises:
the first pair of BGA connectors providing the first differential signal pair to the first pair of vias, and
the second pair of BGA connectors providing the second differential signal pair to the second pair of vias.

23. The method of claim 21, further comprising:
conveying a third differential signal pair, wherein a third pair of vias, which extend through the substrate, convey the third differential signal pair; and
conveying a fourth differential signal pair, wherein a fourth pair of vias, which extend through the substrate, convey the fourth differential signal pair, wherein
the third pair of vias is positioned in a third plane,
the third plane is substantially equidistant from each via in the fourth pair of vias,
the fourth pair of vias is positioned in a fourth plane, and
the fourth plane is substantially equidistant from each via in the third pair of vias.

24. The method of claim 23, wherein
the first pair of vias and the second pair of vias are substantially electromagnetically isolated from the third pair of vias and the fourth pair of vias.

25. The method of claim 21, wherein

a skew of a first pair of traces is matched at a point at which the first pair of traces couples to the first pair of vias.

26. The method of claim 25, wherein
a skew of a second pair of traces is matched at a point at which the second pair of traces couples to the second pair of vias.

27. The method of claim 21, wherein
the conveying the first differential signal pair comprises conveying the first differential signal pair at a data rate greater than 250 megabits per second.

28. A method, comprising:
forming a first pair of vias in a substrate, wherein
the first pair of vias is positioned in a first plane;
forming a second pair of vias in the substrate, wherein
the second pair of vias is positioned in a second plane;
coupling the first pair of vias to receive a first signal pair; and
coupling the second pair of vias to receive a second signal pair, wherein
the first plane is substantially equidistant from each via in the second pair of vias, and
the second plane is substantially equidistant from each via in the first pair of vias.

29. The method of claim 28, wherein
the first signal pair is a first differential signal pair, and
the second signal pair is a second differential signal pair.

30. The method of claim 29, further comprising:
forming a third pair of vias in the substrate, wherein
the third pair of vias is positioned in a third plane;
forming a fourth pair of vias in the substrate, wherein
the fourth pair of vias is located in a fourth plane;

coupling the third pair of vias to receive a third differential signal pair; and

coupling the fourth pair of vias to receive a fourth differential signal pair, wherein

the third plane is substantially equidistant from each via in the fourth pair of vias, and

the fourth plane is substantially equidistant from each via in the third pair of vias.

31. The method of claim 30, further comprising:

substantially electromagnetically isolating the first pair of vias and the second pair of vias from the third pair of vias and the fourth pair of vias.

32. The method of claim 31, wherein

the substantially electromagnetically isolating comprises forming a plurality of isolation vias in the substrate.

33. The method of claim 29, wherein

the coupling the first pair of vias to receive the first differential signal pair comprises coupling the first pair of vias to a pair of Ball Grid Array (BGA) connectors.

34. The method of claim 29, further comprising:

coupling a first differential signal source to the pair of BGA connectors.

35. The method of claim 29, further comprising

matching a first skew of a first pair of traces at a point at which the first pair of traces couples to the first pair of vias.

36. The method of claim 35, further comprising

matching a second skew of a second pair of traces at a point at which the second pair of traces couples to the second pair of vias.

37. The method of claim 36, further comprising
forming the first pair of traces on a same layer as the second pair of traces.

38. An integrated circuit, comprising:
core circuitry configured to process a first signal pair and a second signal pair;
a first pair of leads coupled to the core circuitry and configured to convey the first signal pair; and
a second pair of leads coupled to the core circuitry and configured to convey the second signal pair, wherein
the first pair of leads is positioned in a first plane,
the first plane is substantially equidistant from each lead in the second pair of leads,
the second pair of leads is positioned in a second plane, and
the second plane is substantially equidistant from each lead in the first pair of leads.

39. The integrated circuit of claim 38, wherein
the first signal pair is a first differential signal pair, and
the second signal pair is a second differential signal pair.

40. An apparatus, comprising:
a substrate;
means for conveying a first positive signal;
means for conveying a first negative signal;
means for conveying a second positive signal; and
means for conveying a second negative signal, wherein
the means for conveying the first positive signal, the means for conveying the first negative signal, the means for conveying the second positive signal, and the means for conveying the second negative signal are located in the substrate,
the first positive signal and the first negative signal are comprised in a first signal pair,

the second positive signal and the second negative signal are comprised in a second signal pair,

the means for conveying the first positive signal and the means for conveying the first negative signal are positioned in a first plane,

the first plane is substantially equidistant from the means for conveying the second positive signal and the means for conveying the second negative signal,

the means for conveying the second positive signal and the means for conveying the second negative signal are positioned in a second plane, and

the second plane is substantially equidistant from the means for conveying the first positive signal and the means for conveying the first negative signal.

41. The apparatus of claim 40, wherein

the first signal pair is a first differential signal pair, and

the second signal pair is a second differential signal pair.

42. The apparatus of claim 41, further comprising:

means for generating the first differential signal pair, wherein the means for generating are coupled to the means for conveying the first positive signal and to the means for conveying the first negative signal.

43. The apparatus of claim 41, wherein

the means for conveying the first positive signal and the means for conveying the first negative signal are positioned relative to the means for conveying the second positive signal and the means for conveying the second negative signal such that a crosstalk effect caused by the first signal pair on the second positive signal reduces a crosstalk effect caused by the first signal pair on the second negative signal.

44. The apparatus of claim 43, wherein

the means for conveying the first positive signal and the means for conveying the first negative signal are positioned relative to the means for conveying the second positive signal and the means for conveying the second negative signal such that the crosstalk effect caused by the first signal pair on the second positive signal substantially cancels the crosstalk effect caused by the first signal pair on the second negative signal.